REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 106-110, 112-116, 119-120, 123, 126-129, 131 and 136-140 are pending, wherein Claims 106, 110, 113-116, 120 and 131 are currently amended, Claims 136-140 are newly added, and Claims 1-105, 111, 117, 118, 121, 122, 124, 125, 130 and 132-135 are canceled.

Applicants added the subject matter that "a passivation layer comprises an inorganic material" into claims 106 and 120. The amendment should add no new matters. Applicants teach that the passivation layer may comprise PECVD oxide, PECVD nitride, silicon nitride, silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), or borophosphosilicate glass (BPSG), which can be deemed as an inorganic material. ~ *See lines 9-11 of the 2nd paragraph in page 10, the last paragraph in page 18, and the first paragraph in page 18 of the original specification* ~

Applicants amended the top limit of 100 microns to that of 15 microns in claim 120 to overcome Seppala et al's reference, US5,665,639. The amendment should add no new matter because the range of between 2 and 15 microns is within that of between 2 and 100 microns that is disclosed in lines 3-6 of page 12 in the original specification.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 106-110, 112-116 and 119

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As currently amended, independent claim 106 is recited below:

106. A semiconductor chip or wafer comprising:
a silicon substrate;
a metallization structure over said silicon substrate;
a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure; and
a metal trace over part of said passivation layer and over said first contact pad, wherein said metal trace comprises a gold layer with a thickness of between 2 and 100 μm, wherein said metal trace comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

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Reconsideration of Claims 106-110, 112-116 and 119 rejected under 35 U.S.C. 103(a) as being unpatentable over US6,555,459 to Tokushige et al. in view of US5,665,639 to Seppala et al. is requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 106 patentably distinguishes over the citation by Tokushige et al. (US5,659,201) and Seppala et al. (US5,665,639).

Tokushige et al. teach that a circuitry component comprising a silicon substrate **s**; a metallization structure **1** over said silicon substrate **s**; an insulating layer **3** over said metallization structure **1**, wherein an opening in said insulating layer **3** exposes a first contact pad of said metallization structure **1**; and a metal trace **6** and **16** over part of said insulating layer **3** and over said first contact pad, wherein said metal trace **6** and **16** comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different. ~ *See FIG. 6* ~

The Examiner considers that the reference numbers **2** or **3** may be deemed as a passivation layer. ~ *See the last paragraph in page 4, in the last Office Action mailed in Apr. 26, 2006* ~ Applicants respectfully traverse the Examiner's opinion. Typically, a passivation layer comprises an inorganic material, such as PECVD oxide, PECVD nitride, silicon nitride, silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), or borophosphosilicate glass (BPSG). ~ *See lines 9-11 of the 2nd paragraph in page 10, the last paragraph in page 18, and the first paragraph in page 18 of the original specification* ~ Tokushige et al. teach that the insulating layer **3** is made of an epoxy resin or a polyimide resin, which is not an inorganic material. Also, Tokushige et al. fail to teach what kind of the insulating layer **2** may be, and fail to teach the insulating layer **2** may comprise an inorganic layer. Therefore, applicants consider that Tokushige et al. fail to show which element is a passivation layer comprising an inorganic layer, as claimed in claim 106.

Furthermore, The Examiner considers that the insulating layer **2** is over the metallization structure **1**. ~ *See the last paragraph in page 4, in the last Office Action mailed in Apr. 26, 2006*

~ Applicants respectfully traverse the Examiner's opinion. The insulating layer **2** is not over the metallization structure **1** but under the metallization structure **1**.

Furthermore, Tokushige et al. fail to teach the metal trace **6** and **16** may comprise gold, but teach that the metal trace **6** and **16** comprise copper. ~ See lines 33-36, col. 5 ~

The Examiner considers that "Seppala discloses a method for fabricating a circuitry component comprising a thick gold layer 32, fig. 2, with a thickness of between 2 and 100 microns, col. 7 line 12. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use thickness of gold layer teaching of Seppala with Koike's method, because it would have created a more reliable and durable interconnect between the bump and the bonding pad as aught by Seppala, see abstract. Also, it would have been obvious to one of ordinary skill in art to use the thick gold layer teaching Koike and Seppala in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation." *~ See lines 8-18 of page 5, in the last Office Action mailed in Apr. 26, 2006 ~*

The Examiner's opinions make the applicants confused because Examiner does not clearly explain the relationship between Koike's method and the claims, and does not explain how Seppala et al.'s gold bump can be combined with Koike's method to obtain claim 106.

Seppala et al. teach a gold bump having a gold layer **240** with a thickness of 25 microns. *~ See Fig. 3d and lines 12-15, col. 7 ~* However, Seppala et al. fail to teach a metal trace may

have a gold layer with a thickness of 25 microns. Those skilled in the art should not come up with a metal trace comprising a gold layer, as claimed in claim 106, because Seppala et al. fail to teach the concept of a gold layer **240** with a thickness of 25 microns may be applied to forming a metal trace over a passivation layer comprising an inorganic material.

Applicant considers that the subject matter that "a metal trace comprising a gold layer with a thickness of between 2 and 100 microns is over a passivation layer comprising an inorganic material" should be patentable, because no one teaches the subject matter. Therefore, applicants respectfully submit independent claim 106 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 107-110, 112-116 and 119 patently define over the prior art as well.

Response to Claims 120, 123, 126-129, and 131

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As currently amended, independent claim 120 is recited below:

120. A semiconductor chip or wafer comprising:
a silicon substrate;
a metallization structure over said silicon substrate;
a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; and
a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 15 μm and is used to be wirebonded thereto.

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Reconsideration of Claims 120, 126-129 and 131 rejected under 35 U.S.C. 102(b) as being anticipated by US5,665,639 to Seppala et al. and of Claim 123 rejected under 35 U.S.C. 103 (a) as being unpatentable over US5,665,639 to Seppala et al. in view of US6,555,459 to Tokushige et al. is requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 120 patentably distinguishes over the citation by Seppala et al. (US5,665,639).

Seppala et al. teach that a circuitry component comprises a silicon substrate **200**; a metallization structure **211** over said silicon substrate **200**; a passivation layer **220** over said metallization structure **211**, wherein an opening in said passivation layer **220** exposes a first contact pad of said metallization structure **211**, and wherein said passivation layer **220** comprises an inorganic material; and a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer **240** is used to be wirebonded thereto. ~ *See Fig. 3d, lines 12-15, col. 7 and line 1, col. 10* ~

Seppala et al. teach a gold bump having a gold layer **240** with a thickness of 25 microns. ~ *See Fig. 3d and lines 12-15, col. 7* ~ However, Seppala et al. fail to teach a metal pad having a gold layer with a thickness as thin as between 2 and 15 microns can be used to be wirebonded thereto, as claimed in claim 120. Seppala et al. fail to teach the gold layer **240** may be as thin as between 2 and 15 microns so that the cost for forming the gold layer **240** is higher than that for forming the gold layer with a thickness as thin as between 2 and 15 microns as claimed in claim 120. Applicants find the contact pad comprising a gold layer with a thickness as thin as between

2 and 15 μm can be used to be wirebonded thereto with a good quality, which is not taught by Seppala et al.

For at least the foregoing reasons, applicants respectfully submit independent claim 120 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 123, 126-129, and 131 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Le not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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